

10/082517
02/22/02

PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10082517	FILING DATE 02/22/2002	CLASS 438	SUBCLASS 4	GAU 2812	EXAMINER T.R.S. Dinyan
----------------------	---------------------------	--------------	---------------	-------------	---------------------------

**APPLICANTS: Sanchez Reno; Thorpe Douglas;

**CONTINUING DATA VERIFIED:

BEST AVAILABLE COPY

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH <input checked="" type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	35 USC 119 conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	ATTORNEY DOCKET NO X-998 US
Verified and Acknowledged Examiners's initials H-1		
TITLE : Method and system for inserting probe points in FPGA-based system-on-chip (SoC)		
U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)		

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Assistant Examiner	Total Claims
ISSUE FEE			Print Claim for O.G.
Amount Due	Date Paid	Primary Examiner	DRAWING
			Sheets Drwg. Figs. Drwg. Print Fig.
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner
WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.			

FILED WITH:

☐ DISK (CRF)

☐ CD-ROM

(Attached in pocket on right inside flap)